Ultra-Broad-Band GaAs Monolithic Amplifier

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Abstract—GaAs monolithic IC design and fabrication techniques suitable for baseband pulse amplification have been developed. The developed GaAs monolithic amplifier has a two-stage construction using two source-grounded FET's. To reduce input VSWR without serious noise-figure degradation, an inter-gate-drain negative feedback circuit was adopted. An interstage circuit is a dc-coupled circuit consisting of an appropriate impedance transmission line. Gate voltage for the second-stage FET is self-biased. The amplifier has 13.5-dB gain over the 3-dB bandwidth from below 500 kHz to 2.8 GHz. Less than 6-dB (7-dB) noise figure was obtained from 700 MHz to 2.2 GHz (150 MHz to 3 GHz). Input VSWR is less than 1.5 (2.5) from 600 kHz to 1.1 GHz (500 kHz to 2.1 GHz). Output VSWR is less than 1.6 from 500 kHz to 4.5 GHz. By introducing a low-pass matching network, high-cutoff frequency for the amplifier could be extended to 4.7 GHz without degrading low-frequency characteristics.

I. Introduction

GIGABIT-PER-SECOND data rate systems need baseband pulse amplifiers which exhibit low input and output VSWR to 50 Ω, as well as high flat gain and low noise figure over the frequency range from several hundred kilohertz to several gigahertz. For instance, a 1.6 Gbit/s optical communication system requires amplifiers having 2-GHz high-cutoff frequency, 100-kHz low-cutoff frequency, less than 7-dB noise figure, and less than 1.5 input VSWR (below 1.6 GHz). To achieve these requirements, hybrid IC techniques, using discrete GaAs FET's, have been used [1]. However, to realize lower cost and higher reliability, development of a GaAs monolithic IC technique suitable for the baseband pulse amplification is necessary. For GaAs monolithic baseband pulse amplifiers, more sophisticated design techniques are required than for IF amplifiers [2] or other general purpose amplifiers [3], [4], [12].

This paper describes design considerations and performances for a newly developed GaAs monolithic amplifier, intended primarily for use as a baseband pulse amplifier in gigabit-per-second data rate systems [13].

The developed GaAs monolithic amplifier has a two-stage construction using two source-grounded FET's. To reduce input VSWR without serious noise-figure degradation, an inter-gate-drain negative feedback circuit and a 400-μm gate-width FET were used for the first stage. A dc-coupled circuit, consisting of a high impedance transmission line, was adopted for the interstage circuit. Gate dc bias voltage for the second-stage FET is self-biased. The developed amplifier has 13.5-dB gain over the 3-dB bandwidth from below 500 kHz to 2.8 GHz. Input VSWR is less than 1.5 (2.5) from 600 kHz to 1.1 GHz (500 kHz to 2.1 GHz). Output VSWR is less than 1.6 from 500 kHz to 4.5 GHz. Noise figure is less than 6 dB (7 dB) from 700 MHz to 2.2 GHz (150 MHz to 3 GHz). By introducing a low-pass external matching network, the high-cutoff frequency for the amplifier could be extended to 4.7 GHz without degrading low-frequency characteristics.

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II. Circuit Design

A. Bandwidth and Noise Figure

To obtain more than 15-dB gain in a 50-Ω system, two-stage construction is necessary. In this section, assuming a fixed gate width (400 μm) for the second-stage FET, relations between the first-stage FET gate width and gain-bandwidth, related with noise figure, are discussed.

The load resistance for the second-stage FET becomes 33 Ω when the drain bias voltage is supplied through a 100-Ω resistor, since the load resistance for the amplifier is 50 Ω. If gain for the second-stage FET is designed at 6 dB, an FET transconductance g_m of 60 mS is needed. The 60 mS transconductance is obtained by a recessed gate GaAs MESFET having a 400-μm gate width. Meanwhile, in the two-stage amplifier, the high-cutoff frequency is restricted mainly by the second-stage FET input capacitance.

Using y-parameters for a source-grounded intrinsic FET [5], voltage gain A_v for the first stage can be roughly approximated as

$$A_v = \frac{-y_{21}}{\frac{1}{Z_L} + y_{22}} = \frac{-g_m + j\omega C_{DG}}{\frac{1}{R_L} + j\omega C_I + G_d + j\omega C_{DG}} \simeq \frac{-g_m R_L}{1 + j\omega R_L C_I} \tag{1}$$

where Z_L is the load impedance for the first-stage FET, R_L is the load resistance for the first-stage FET, G_d is the drain conductance for the first-stage FET, and C_I is the input capacitance for the second-stage (mainly the source-gate capacitance C_{SG} for the second-stage FET). In GaAs FET's, the drain-gate capacitance C_{DG} is negligible, compared with the C_{SG} under first-order approximation [5]. Therefore, when gate widths for the first-stage and the second-stage FET's are not so different, $C_I \gg C_{DG}$ is also obtained.

From (1), high-cutoff frequency (3-dB bandwidth) f_c and

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	Gain for the first-stage	high-cutoff frequency	noise figure (dB)
(a)	$-g_m R_L$	$\frac{1}{2\pi R_L C_I} \cdot \frac{1}{n}$	$10(\log n + \log \frac{KG_s}{g_m})$
(b)	$-g_m R_L$	$\frac{1}{2\pi R_L C_I}$	$10 \log \frac{KG_s}{g_m}$

Wg : gate width

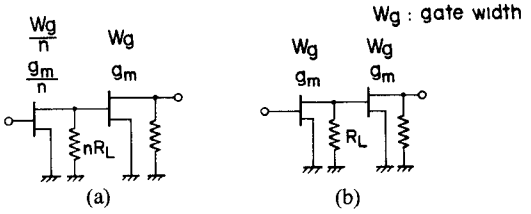

Fig. 1. Gate-width dependence on bandwidth and noise figure.

flat gain A_{v0} are

$$f_c \simeq \frac{1}{2\pi R_L C_I} \tag{2}$$

$$A_{v0} \simeq -g_m R_L. \tag{3}$$

Meanwhile, the noise figure F for the amplifier is approximated as follows [1], [6]:

$$F = F_0 + \frac{R_n}{G_s}\left[(G_s - G_0)^2 + B_0^2\right]$$

$$\simeq F_0 + R_n G_s \tag{4}$$

where G_S is the source conductance, F_0 is the minimum noise figure for the amplifier, $G_0 + jB_0$ is the optimum source admittance which gives F_0, and R_n is the equivalent noise resistance. In (4), approximate relations $G_s \gg G_0$ and $B_0 \simeq 0$ are also used [1]. From Fukui's work [7], R_n is represented as

$$R_n = \frac{K}{g_m} \quad (K = \text{const.}). \tag{5}$$

Substituting (5) into (4), the following formula is obtained:

$$F \simeq F_0 + \frac{KG_s}{g_m} \approx \frac{K}{g_m} G_s. \tag{6}$$

Using (2), (3), and (6), gain, high-cutoff frequency, and noise figure for the amplifier constructions shown in Fig. 1 can be calculated. The results are also shown in Fig. 1.

Thus, bandwidth and noise figure for the ultra-broadband amplifier depend largely on the gate width for the first-stage FET. In this work, the gate widths, for both first-stage and second-stage FET's, were chosen as 400 μm ($n = 1$), considering cascade connection for amplifier chips.

B. Input VSWR Reduction

To reduce input VSWR for MESFET's, three methods, shown in Fig. 2 are known.

Method 1: An input impedance for a source-grounded MESFET is very high compared with 50 Ω in the low-frequency range (below 1 GHz). Therefore, by connecting a 50-Ω resistor R_I parallel to the input port, low VSWR

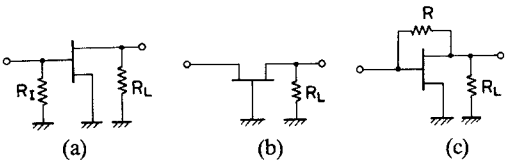

Fig. 2. Circuit configurations for input VSWR reduction.

can be achieved (Fig. 2(a)). However, this method degrades the noise figure by about 6 dB [1].

Method 2: Input admittance for a gate-grounded FET in the low-frequency range is represented as

$$Y_{\text{in}} = g_m + G_d - \frac{(g_m + G_d)G_d}{\frac{1}{R_L} + G_d}. \tag{7}$$

Y_{in} depends on g_m, G_d, and R_L. In this case (Fig. 2(b)), by choosing a 140-μm gate width ($b_m = 21$ mS, $G_d = 1.2$ mS), $Y_{\text{in}} = 20$ mS (VSWR = 1) is obtained (when $R_L = 100$ Ω). Both the source-grounded and the gate-grounded FET's have nearly the same noise figure for the same source admittance [8]. This results in a 4.5-dB noise-figure degradation, compared to the source-grounded 400-μm gate-width FET ((6)).

Method 3: By using an inter-gate-drain negative feedback, input VSWR can be reduced [9] (Fig. 2(c)). In this case, the low frequency input admittance Y_{in} is given by

$$Y_{\text{in}} = \frac{1}{R} + \frac{\frac{1}{R}\left(g_m - \frac{1}{R}\right)}{\frac{1}{R_L} + G_d + \frac{1}{R}} \tag{8}$$

where R is the feedback resistor. Generally, the noise figure F_T for noisy two-port circuits connected in parallel can be expressed as follows:

$$F_T = 1 + \sum_{i=1}^{n} (F_i - 1) \tag{9}$$

where F_i is the noise figure for the parallel circuit in which only the ith two-port circuit includes noise sources (the others are noise free), and where n is the positive integer, which means the number of noisy two-port circuits (see Appendix I). Using (9), noise-figure degradation due to the negative feedback resistor in Fig. 2(c) (when FET gate width is 400 μm) is estimated as 2 dB (see Appendix II). The lowest noise figure can be obtained by Method 3.

Consequently, the inter-gate-drain negative feedback method is the most suitable for the low noise ultra-broadband GaAs monolithic amplifier.

C. Circuit Configuration

Fig. 3(a), (b), and (c) show equivalent circuits for three variational uses of the developed GaAs monolithic amplifier. In the figure, an enclosed block with a broken line was fabricated on a single GaAs chip. In GaAs monolithic IC's, capacitor fabrication for more than 50-pF capacitance is difficult from a practical point of view. Therefore, to extend the low-cutoff frequency below 10 MHz, the intro-

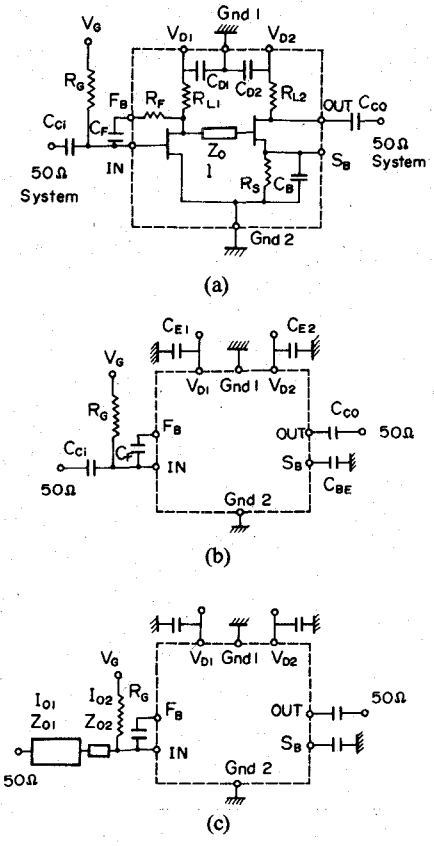

Fig. 3. Equivalent circuits for three variational uses of the developed GaAs monolithic amplifier. (a) IF amplifier. (b) Baseband pulse amplifier. (c) Baseband pulse amplifier with external matching.

duction of a dc-coupled circuit is necessary. In addition to this, coupling capacitors in the IC have parasitic parallel capacitances which degrade the high-cutoff frequency. Accordingly, in this work, a dc-coupled circuit, which consists of a high impedance transmission line, was adopted for the interstage circuit to accomplish the broad-band performance. To reduce input VSWR without serious noise-figure degradation, an inter-gate-drain negative feedback circuit was adopted for the first-stage FET. Gate dc voltage for the second-stage FET is self-biased. The circuit shown in Fig. 3(a) has a low-cutoff frequency of 250 MHz, which is due to C_B (12 pF). A high-cutoff frequency for the circuit (Fig. 3(a)) is 3 GHz. Therefore, the circuit shown in Fig. 3(a) is suitable for the IF amplifier in microwave systems. When using the chip for the baseband pulse amplification, multilayer ceramic-chip capacitors C_{E1}, C_{E2}, and C_{BE} should be added, as shown in Fig. 3(b). Gain (S_{21}), VSWR versus frequency characteristics for Fig. 3(b), simulated using S parameters measured for a 400-μm gate-width discrete FET, has a 3-dB bandwidth of 350 kHz–3 GHz with 14-dB gain. Simulated input VSWR is less than 1.5 (2) from 1 MHz to 1 GHz (600 kHz–1.6 GHz) and output VSWR is less than 1.7 from below 500 kHz to 3 GHz. Low-cutoff frequency is due to dc block capacitors and RF bypass capacitors outside the chip (15000 pF).

By introducing a low-pass external matching circuit at the input port, as shown in Fig. 3(c), simulated high-cutoff frequency can be extended to 4.8 GHz without degrading low-frequency characteristics. A low-pass matching circuit operates as a circuit having short electrical length in the low-frequency range [1].

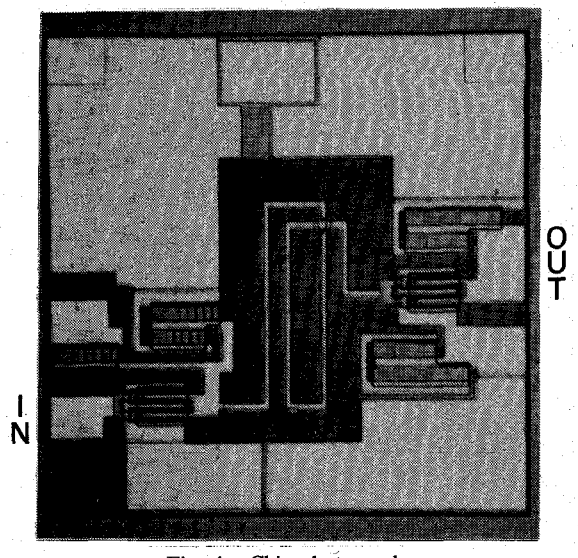

Fig. 4. Chip photograph.

III. Device Fabrication

The wafers used have a GaAs epitaxial layer with a 2.3×10^{17} cm^{-3} carrier concentration. Fig. 4 shows a chip photograph. Chip size is 1.1-mm square.

A. FET

In the amplifier, MESFET's fabricated on the epitaxial layer have a 1.2-μm gate length, a 400-μm gate width, and a 100-μm gate finger length. The Schottky barrier gate (Ti–Al–Ti) was formed by a lift-off technique. The gate region of the channel was recessed. The recessed depth is about 600 Å. Ohmic contacts were prepared by alloying a Au–Ge–Ni film. Pinchoff voltage $V_p = 2$ V, drain saturation current $I_{DSS} = 90$ mA, and $g_m = 50$ mS were obtained for 400-μm gate width.

B. Resistor

Resistors are fabricated by the epitaxial layer thinned to about an 1800-Å uniform thickness by an anodic oxidation technique. The large state density at the GaAs surface brings about a depletion layer extending from the surface into the channel [10], resulting in larger resistance than without considering the surface depletion layer. Sheet resistance $R_\square$ for the resistors is represented using electron charge e, carrier concentration n, electron mobility μ, epitaxial layer thickness d, and surface depletion layer thickness d' as

$$R_\square = \frac{1}{en\mu(d-d')}. \tag{10}$$

The fabricated resistor has 625-Ω/□ sheet resistance. Using (10), d' is calculated as 700 Å, where an electron mobility $\mu = 4000$ [cm^2/Vs] is used.

When internal electric fields in GaAs reach the critical field (3 kV/cm), causing saturation electron velocity, the

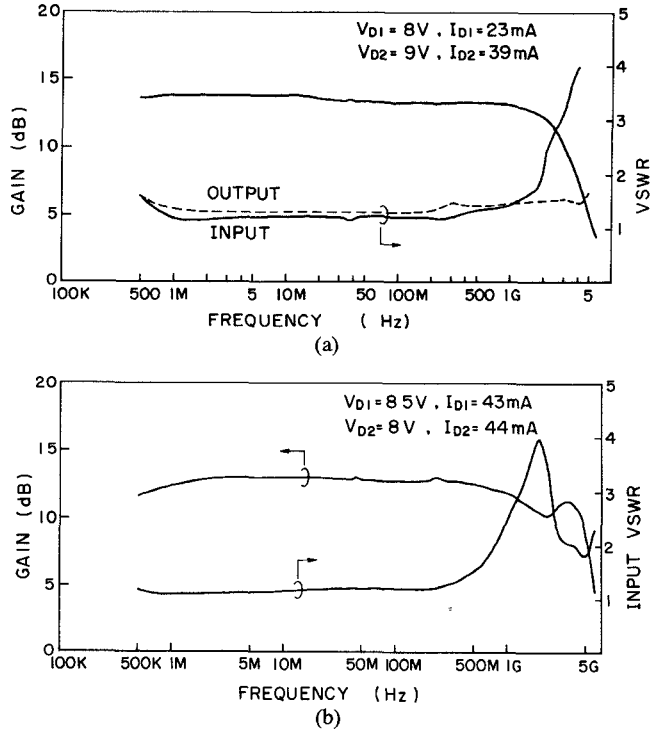

Fig. 5. Gain, VSWR versus frequency characteristics for the GaAs ultra-broad-band amplifier (a) without external matching and (b) with external matching.

GaAs epitaxial layer cannot be used for linear resistors. In the developed amplifier, resistors are 30-μm long. Since voltage drops across the resistors are within 5.5 V even at 3 $V_{p\text{-}p}$ output voltage swing, the maximum internal electric field is 1.83 kV/cm. Therefore, the resistors can be used under linear operation.

C. Capacitor

Metal-insulator-metal (MIM) capacitors were fabricated on a semi-insulating GaAs substrate, where the insulator is a 2000-Å thick CVD–SiO_2 film. The first and the second level metal systems for the capacitors are Ti–Al–Ti and Ti–Pt–Au, respectively.

D. Transmission Line

A relatively high impedance microstrip transmission line for direct coupling was fabricated on the chip. The microstrip conductor was formed from Ti–Al–Ti–Pt–Au. Its width is 17 μm. GaAs chip thickness is 150 μm. Characteristic impedance for the transmission line is about 80 Ω.

IV. Performance

Completed circuits are mounted on a microstrip test fixture. Gain (S_{21}), VSWR versus frequency characteristics for the amplifier, measured in a 50-Ω system, are shown in Fig. 5(a) and (b). Fig. 5(a) and (b) correspond to Fig. 3(b) and (c), respectively.

The amplifier without external matching has 13.5-dB gain over the 3-dB bandwidth from below 500 kHz to 2.8 GHz, as shown in Fig. 5(a). Input VSWR is less than 1.5 (2.5) from 600 kHz to 1.1 GHz (500 kHz to 2.1 GHz). Output VSWR is less than 1.6 from 500 kHz to 4.5 GHz.

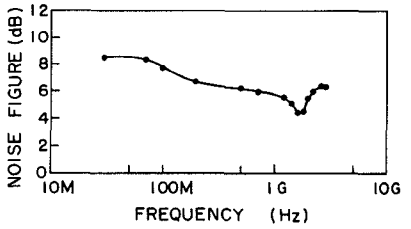

Fig. 6. Noise figure without external matching.

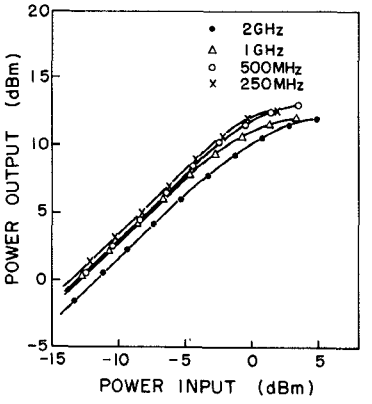

Fig. 7. Input–output power responses for an amplifier without external matching.

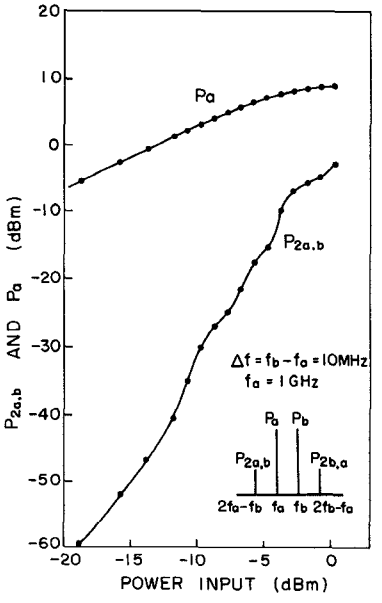

Fig. 8. Third-order intermodulation.

By introducing a low-pass external matching network, high-cutoff frequency for the amplifier could be extended to 4.7 GHz without degrading low-frequency characteristics.

The noise figure without external matching is less than 6 dB (7 dB) from 700 MHz to 2.2 GHz (150 MHz to 3 GHz), as shown in Fig. 6. Fig. 7 shows input–output power responses for the amplifier without external matching, measured at 250 MHz, 500 MHz, 1 GHz, and 2 GHz, respectively. As seen in the figure, 10-dBm power output is obtained at 1-dB gain compression over the frequency range. Third-order intermodulation distortion (IMD3), measured at 1 GHz by injecting two equal amplitude

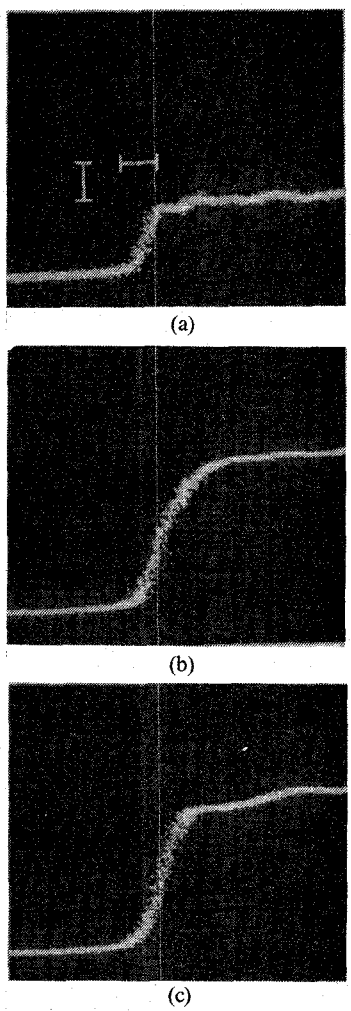

Fig. 9. Amplifier step responses. (a) Input waveform. V: 100 mV/div; H: 100 ps/div. (b) Output waveform without external matching. V: 200 mV/div; H: 100 ps/div. (c) Output waveform with external matching. V: 200 mV/div; H: 100 ps/div.

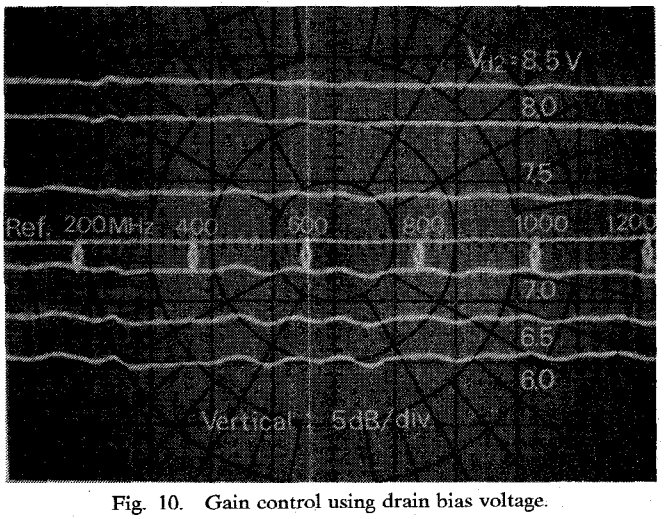

Fig. 10. Gain control using drain bias voltage.

signals separated in frequency by 10 MHz, is shown in Fig. 8. When total power for the two injecting signals is 0 dBm (10 dBm), IMD3 value is 50 dB (23 dB).

Fig. 9(a), (b), and (c) show an input step waveform having 10-percent to 90-percent risetime of 75 ps, an output waveform without external matching, and an output waveform with external matching, respectively. As seen in the figure, the amplifier can be used as the gigabit baseband pulse amplifier. It can also be seen that, by adding the external matching network, step response risetime is improved. The amplifier gain can be controlled by drain bias voltage, as shown in Fig. 10. Gain control over 22 dB was observed without frequency dependence, from 100 MHz to 1200 MHz.

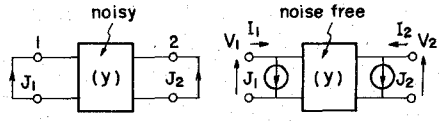

Fig. 11. Noisy two-port circuit representation.

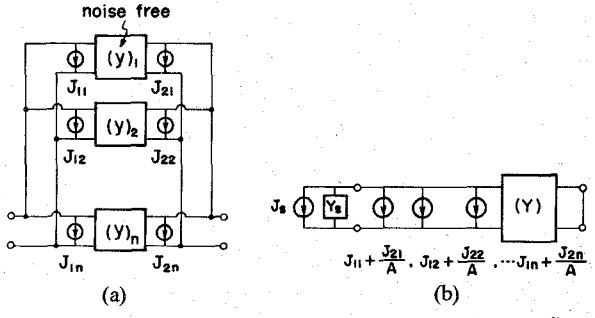

Fig. 12. (a) Parallel connection for noisy two-port circuits. (b) Current noise sources replacement at the output port into the input port.

V. Conclusion

GaAs monolithic IC techniques suitable for baseband pulse amplification have been developed. Design considerations on bandwidth, noise figure, and input VSWR reduction were discussed. In the developed amplifier, the inter-gate-drain negative feedback was adopted to reduce input VSWR without serious noise-figure degradation. The interstage circuit is a dc-coupled circuit consisting of an appropriate impedance transmission line. The developed amplifier has 13.5-dB gain over the 3-dB bandwidth from below 500 kHz to 2.8 GHz. Less than 6-dB (7-dB) noise figure was obtained over the 700-MHz to 2.2-GHz (150-MHz to 3-GHz) frequency range. Input VSWR is less than 1.5 (2.5) from 600 kHz to 1.1 GHz (500 kHz to 2.1 GHz). Output VSWR is less than 1.6 from 500 kHz to 4.5 GHz. By introducing a low-pass matching network, high-cutoff frequency for the amplifier could be extended to 4.7 GHz without degrading low-frequency characteristics. The developed monolithic amplifier will be used in gigabit data rate systems, such as ultra-high-speed optical communication and PCM communication systems.

Appendix I

Noise Figure for Parallel Two-Port Circuits

As shown in Fig. 11, internal noise sources are represented by sources of current flowing in parallel both with input current I_1 and output current I_2. In a parallel circuit containing noisy two-port circuits shown in Fig. 12(a), the

noise current sources at the output port can be replaced in the input port, using short-circuit current gain for the parallel circuit, as shown in Fig. 12(b). In the figure, y-parameters (Y) and short-circuit current gain A for the parallel circuit are

$$Y=\begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix}=\begin{pmatrix} \sum_{i=1}^{n} y_{11i} & \sum_{i=1}^{n} y_{12i} \\ \sum_{i=1}^{n} y_{21i} & \sum_{i=1}^{n} y_{22i} \end{pmatrix} \tag{A1}$$

$$A=\frac{-Y_{21}}{Y_s+Y_{11}} \tag{A2}$$

where Y_S is the source admittance.

In Fig. 12(b), J_{1i} and J_{2i} are correlated. There are no correlations between J_{1i}, J_{2i} and J_{1j}, J_{2j} $(i \neq j)$.

Here, noise current spectral density S_{Ni} is defined as

$$S_{Ni}=\overline{\left|J_{1i}+\frac{J_{2i}}{A}\right|^2}. \tag{A3}$$

Source current spectral density S_S is

$$S_s=\overline{J_s^2}=4kT\,\mathrm{Re}(Y_s). \tag{A4}$$

Using (A3) and (A4), noise figure F_T for the parallel circuit is written as follows:

$$F_T=1+\sum_{i=1}^{n} S_{Ni}/4kT\,\mathrm{Re}(Y_s). \tag{A5}$$

J_{1i} can be split into two components, one completely correlated $(J_{1i}-J_{1iu})$ with J_{2i} and one uncorrelated J_{1iu} with J_{2i}.

Using these expressions and (A3), S_{Ni} is represented as

$$S_{Ni}=\overline{J_{1iu}^2}+\frac{\overline{J_{2i}^2}}{(+Y_{21})^2}|Y_{ci}+Y_s+Y_{11}|^2 \tag{A6}$$

$$Y_{ci}\equiv\frac{J_{1i}-J_{1iu}}{J_{2i}}(-Y_{21}) \tag{A7}$$

where Y_{ci} is the correlation admittance.

F_i is defined as

$$F_i=1+S_{Ni}/4kT\,\mathrm{Re}(Y_s) \tag{A8}$$

where F_i is the noise figure for the parallel circuit, in which only the ith two-port circuit includes noise sources, while the others are noise free.

From (A5) and (A8), noise figure F_T for the parallel circuit, in which all two-port circuits have noise sources, is written as

$$F_T=1+\sum_{i=1}^{n}(F_i-1). \tag{A9}$$

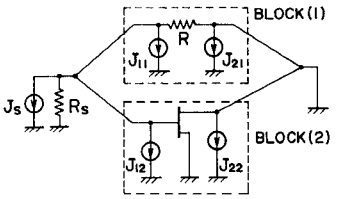

Fig. 13. A noise equivalent circuit for a source-grounded FET with the inter-gate-drain negative feedback.

Appendix II

Noise Figure for Negative Feedback Amplifier

Short-circuit current gain A_F in low-frequency range for the circuit shown in Fig. 13 is

$$A_F=-\left(g_m-\frac{1}{R}\right)\Big/\left(\frac{1}{R_s}+\frac{1}{R}\right). \tag{A10}$$

In the figure, J_{11} and J_{21} are fully correlated since J_{11} and $-J_{21}$ are the same current. Therefore, correlation admittance Y_{c1} for block (1) in Fig. 13 becomes

$$Y_{c1}=Y_{21}=g_m-\frac{1}{R}. \tag{A11}$$

From (A5), noise figure F_1 for the circuit, in which only block (1) has noise sources, is

$$F_1=1+\frac{\left|\frac{1}{R_s}+g_m\right|^2 R_s}{\left(g_m-\frac{1}{R}\right)^2 R}=1.41 \tag{A12}$$

where values of $g_m=60$ mS (400-μm gate width) and $R=250\ \Omega$ are used. Defining noise figure F_2 for the circuit in which only block (2) has noise sources, and noise figure F_N for the FET without the feedback resistor (block (1)), $(F_1-1)/(F_N-1)$ is replaced by

$$\frac{F_2-1}{F_N-1}=\frac{\overline{J_{12u}^2}+\left|J_{12}-J_{12u}+\dfrac{J_{22}}{-\sum_{1}^{2} y_{21i}\Big/\left(Y_s+\sum_{1}^{2} Y_{11i}\right)}\right|^2}{\overline{J_{12u}^2}+\left|J_{12}-J_{12u}+\dfrac{J_{22}}{-y_{21}/(Y_s+y_{11})}\right|^2}. \tag{A13}$$

In short-channel GaAs MESFET's, J_{12} and J_{22} can be approximately treated as fully correlated [11].

To examine J_{12} and J_{22} magnitude, a Q value defined by

(A14) was measured:

$$Q \equiv \frac{F_{N,25}-1}{F_{N,50}-1} = \frac{1}{2} \cdot \frac{\left|J_{12}+\dfrac{J_{22}}{(-y_{21}/0.04)}\right|^2}{\left|J_{12}+\dfrac{J_{22}}{(-y_{21}/0.02)}\right|^2} \quad \text{(A14)}$$

where $F_{N,25}$ is the FET noise figure for 25-Ω source impedance and F_{N50} is the FET noise figure for 50-Ω source impedance (without feedback). Measured Q value was 2.5. In (A14), if J_{22} is neglected, the Q value becomes 0.5. On the other hand, if J_{12} is neglected, the Q value becomes 2. Therefore, it is considered that J_{22} is more dominative than J_{12}. Assuming $J_{12u}=0$ and $J_{12}=0$, (A13) is approximately calculated as

$$\frac{F_2-1}{F_N-1} \approx 1.65. \quad \text{(A15)}$$

Since the measured F_N $(=F_{N,50})$ value for a 400-μm gate-width FET was 2.8 (4.5 dB), F_2 is

$$F_2 \approx 4. \quad \text{(A16)}$$

Consequently, the noise figure for Fig. 13 is obtained from the values for F_1 and F_2, using (A9)

$$F_T = 1+\sum_{i=1}^{2}(F_i-1) \approx 1+0.41+3 = 4.4 \quad (=6.4\ \text{dB}) \quad \text{(A17)}$$

where F_T is about 2 dB higher than F_N (4.5 dB).

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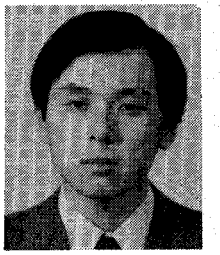

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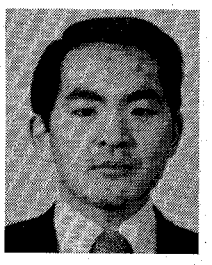

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